New SVPWM to Attack the Gates of Multilevel Inverters (Case Study: PAPF)

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Abstract **-** In this paper, we propose to develop a different control strategy by Pulse Width Modulation (PWM) vector of the three-phase voltage three-level inverter with NPC structure. We start by presenting the structure and model of this converter. Thereafter, we develop the different stages of the algorithm we have implemented. Finally, the results of simulink justifiant fidelity of the model is presented.

Keywords **-** Hysteresis/NSVPWM, Gate, Multilevel Inverter, PAPF, Control, IGBT, MOSFET.

I. INTRODUCTION

Recent standards impose limits on harmonics that a facility can be injected to the grid that feeds. Some solutions exist to meet these requirements: passive filters, magnetic selective cancellation of harmonics by phase shifting transformers, active filters. Another approach is to avoid the source harmonic generation by designing own called rectifiers impose a sinusoidal currents they call the network. These innovative solutions, but very expensive have been used successfully for ballasts for fluorescence and the latest technology in computer power supplies. Unfortunately, these technologies are not yet mature [1].

Voltage inverters are an unavoidable feature of electronics power. They are present in the most diverse areas of application, including best known is probably that of the rate of change of current machines Alternative. The strong evolution of this function is supported, firstly, on the development of fully controllable semiconductor component, powerful, robust, and fast, and secondly, on the almost universal use of techniques known as pulse width modulation [2].

In high power applications, the structure of the three-level inverters is most suitable, as compared to the conventional structure, since the voltages and output currents exhibit a harmonic content much lower. The voltage across each switch is halved and the chopping frequency is lower [1-4].

In this paper, we present in the first part, the structure and the model of the voltage of three-level inverter in NPC structure. Then, in the second part, we present the different stages of the control algorithm by using the Vector PWM 19 voltage vectors the inverter and the simulation results.

Finally, we present experimental results of the application of our inverter on a load RL [3-5].

II. MODEL OF INVERTER A THREE LEVELS

Figure 1 shows the structure of a three-phase voltage to three-level inverter NPC structure. We start by defining the connection function Fki switch. It is 1 if the switch is closed and 0 otherwise.

Incontrollable mode, the inverter connection functions are related by the relation (1) [6-9].

$$\begin{cases} F_{k1} = 1 - F_{k4} \\ F_{k2} = 1 - F_{k3} \end{cases} \quad (1)$$

With k = 1, 2 or 3 and represents the number of arms.

We denote by m = 1: half upper arm and m = 0: The half-arm down.

The potentials of the nodes A, B and C of the three-phase three-level inverter, by relative to the point M is expressed as follows:

$$\begin{cases} V_{AM} = (F_{11}^{b} \times U_{c1}) - (F_{10}^{b} \times U_{c2}) \\ V_{BM} = (F_{21}^{b} \times U_{c1}) - (F_{20}^{b} \times U_{c2}) \\ V_{CM} = (F_{31}^{b} \times U_{c1}) - (F_{30}^{b} \times U_{c2}) \end{cases} \quad (2)$$

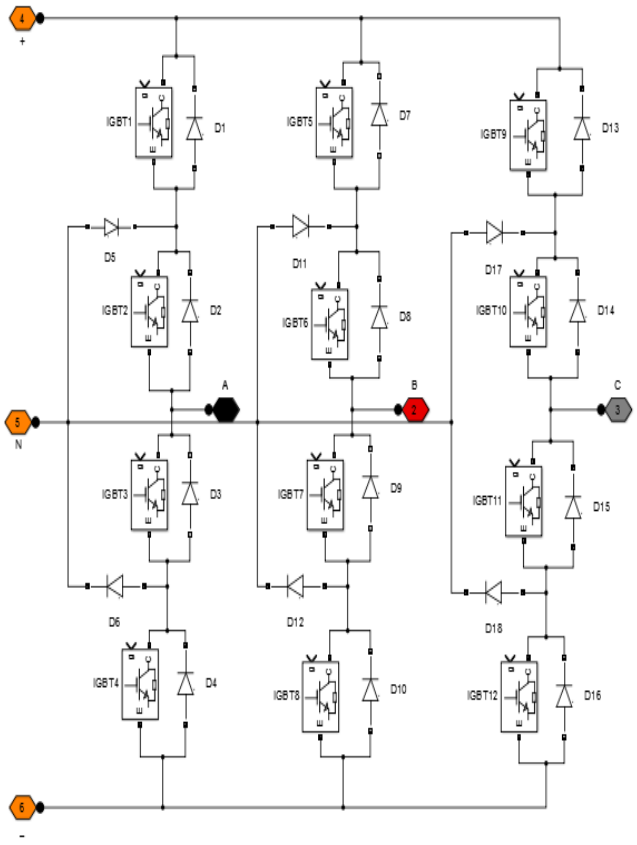

Fig. 1. Three-level inverter with NPC structure

The single output voltages are written:

$$\begin{Vmatrix} V_A \\ V_B \\ V_C \end{Vmatrix} = \frac{1}{3}\begin{vmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{vmatrix} \times \left\langle \begin{vmatrix} F_{11}^b \\ F_{21}^b \\ F_{31}^b \end{vmatrix} U_{c1} - \begin{vmatrix} F_{10}^b \\ F_{20}^b \\ F_{30}^b \end{vmatrix} U_{c2} \right\rangle \qquad (3)$$

III. STRATEGY CONTROL

The strategy proposed in this article is a NSVPWM with Hysterisis can be implemented by the following steps.

- **Step-1:** Determine Ba,Bb and Bc:

Figure 2 shows the outputs voltages Ba,Bb and Bc of a hysterisis.

- **Step-2:** Determine RI(1), RI(2), RI(3), RI(4), RI(5) and RI(6):

From Figure 3, RI(1), RI(2), RI(3), RI(4), RI(5) and RI(6) can be determined as follows:

$$\begin{aligned} R_I(1) &= B_a + \overline{B_b} + \overline{B_c} \\ R_I(2) &= B_a + B_b + \overline{B_c} \\ R_I(3) &= \overline{B_a} + B_b + \overline{B_c} \\ R_I(4) &= \overline{B_a} + B_b + B_c \\ R_I(5) &= \overline{B_a} + \overline{B_b} + B_c \\ R_I(6) &= B_a + \overline{B_b} + B_c \end{aligned} \qquad (4)$$

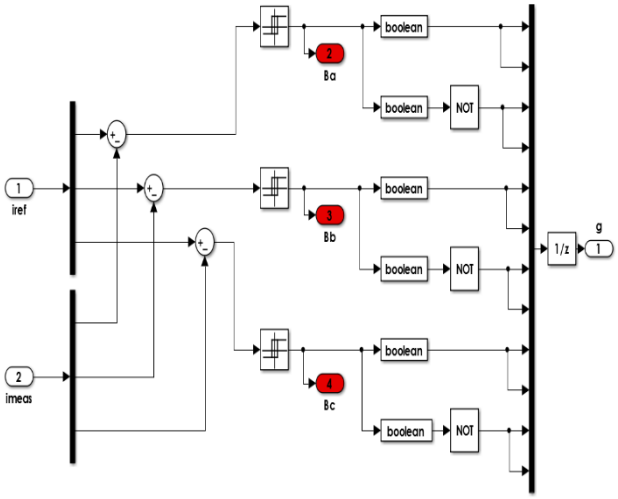

Fig. 2. Outputs voltages Ba,Bb and Bc of a hysterisis.

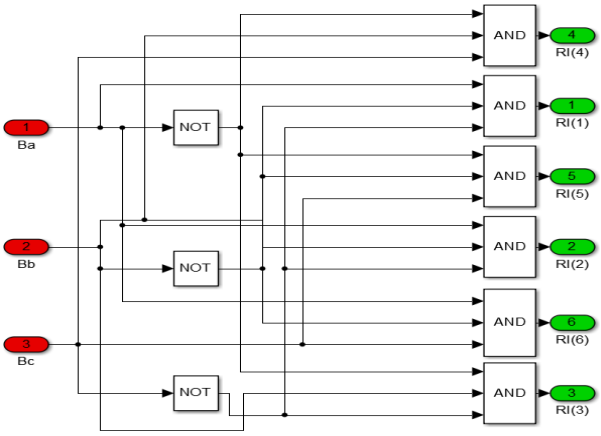

Fig. 3. The outputs : RI(1), RI(2), RI(3), RI(4), RI(5) and RI(6).

- **Step-3:** Determine V*:

From Figure 4, V* can be calculated as follows:

$$V^* = \begin{vmatrix} V_a^* \\ V_b^* \\ V_c^* \end{vmatrix} = U_s + U_f \qquad (5)$$

$$U_f = L_f \frac{du}{dt} \times I_f$$

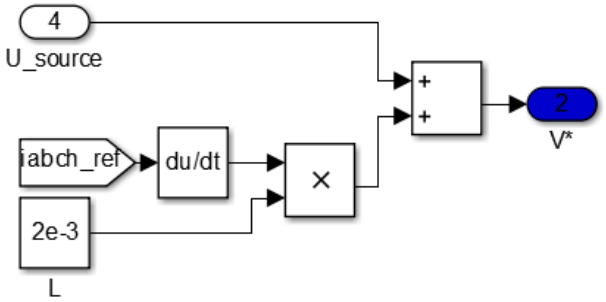

Fig. 4. The output voltage V*.

- **Step-4:** Determine Vab,Vbc,Vca and Xab,Xbc,Xca

$$V_{ab} = V_a^* - V_b^*$$
$$V_{bc} = V_b^* - V_c^* \quad (6)$$
$$V_{ca} = V_c^* - V$$
$$X_{ab}\begin{cases}1\\V_{ab}\cdots X_{bc}\end{cases}\begin{cases}1\\V_{bc}\cdots X_{ca}\end{cases}\begin{cases}1\\V_{ca}\\0\end{cases}$$

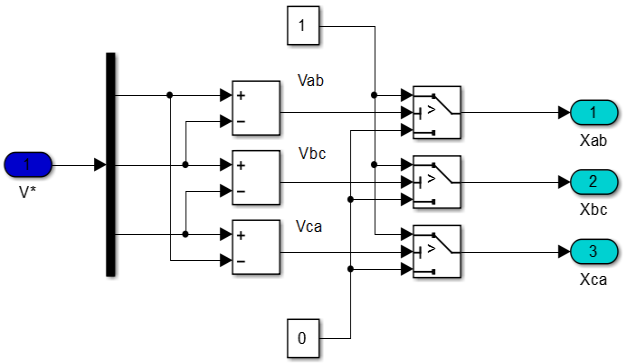

Fig. 5. The outputs : Xab,Xbc and Xca

- **Step-5:** Determine RV(1), RV(2), RV(3), RV(4), RV(5) and RV(6)

From Figure 6, RV(1), RV(2), RV(3), RV(4), RV(5) and RV(6) can be determined as follows:

$$R_V(1) = X_{ab} + X_{bc} + \overline{X_{ca}}$$
$$R_V(2) = \overline{X_{ab}} + X_{bc} + \overline{X_{ca}}$$
$$R_V(3) = \overline{X_{ab}} + X_{bc} + X_{ca} \quad (7)$$
$$R_V(4) = \overline{X_{ab}} + \overline{X_{bc}} + X_{ca}$$
$$R_V(5) = X_{ab} + \overline{X_{bc}} + X_{ca}$$
$$R_V(6) = X_{ab} + \overline{X_{bc}} + \overline{X_{ca}}$$

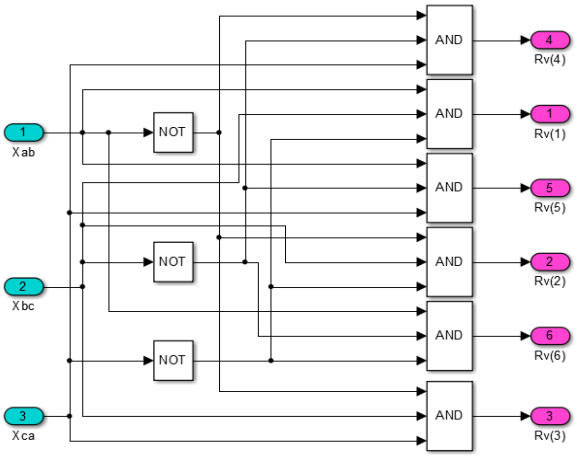

Fig. 6. The outputs : RV(1), RV(2), RV(3), RV(4), RV(5) and RV(6)

- **Step-6:** generating of the inverter switching pulses

Figure 7 shows the NSVPWM pulses to attack the gates of multilevel inverters

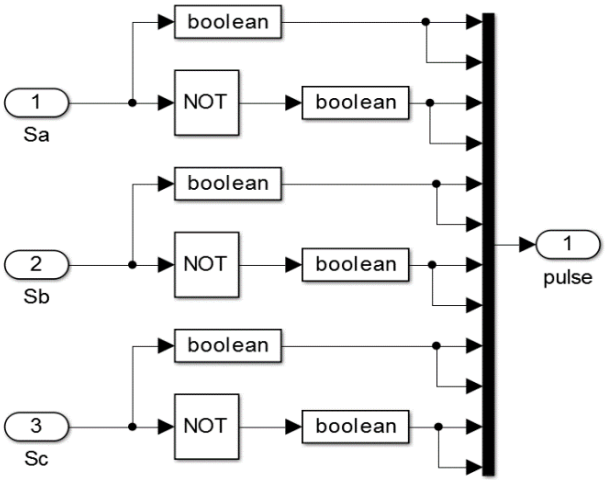

Fig. 7. The output pulses to attack the gates of multilevel inverter

The block diagram of NSVPWM is shown in Figure 8.

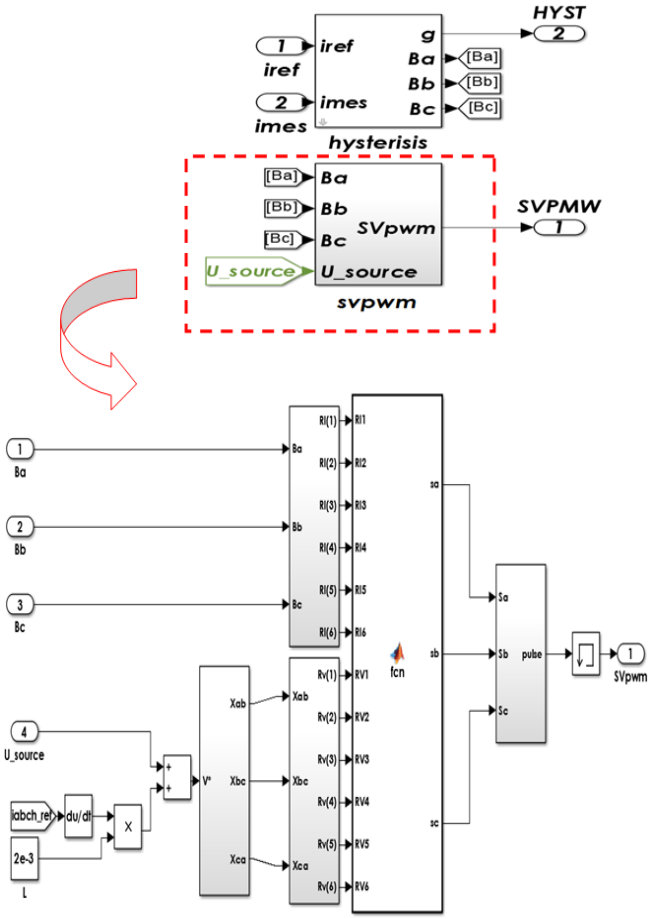

Fig. 8. Block diagram of NSVPWM.

IV. RESULTS AND DISCUSSIONS

The main aim of any modulation technique is to obtain variable output having maximum fundamental component with minimum harmonics. The objective of Pulse Width Modulation techniques is enhancement of fundamental output voltage and reduction of harmonic content in Three Phase Voltage Source Inverters.

In this paper different PWM techniques are compared in terms of Total Harmonic Distortion (THD).

Simulink Models has been developed for Sinusoidal PWM (NSPWM), Space vector PWM (SVPWM), and Space vector PWM switching Patterns. Simulation work is carried in MATLAB 2013/Simulink.

The simulation parameters used are:

- Fundamental frequency 50 Hz
- Switching frequency 20 kHz
- DC voltage 800 Volt
- ODE Solver ode45tb

▪ *Simulation of NSPWM*

Space vector PWM is an advanced technique used for variable frequency drive applications. It utilizes dc bus voltage more effectively and generates less THD in the Three Phase Voltage Source Inverter. SVPWM utilize a chaotic changing switching frequency to spread the harmonics continuously to a wide band area so that the peak harmonics can be reduced greatly.

The load current (Il),PAPF current (If), supply voltage (Us),supply current (Is) and Vdc bus voltage of the PAPF are depicted in figure 9 to figure 13.

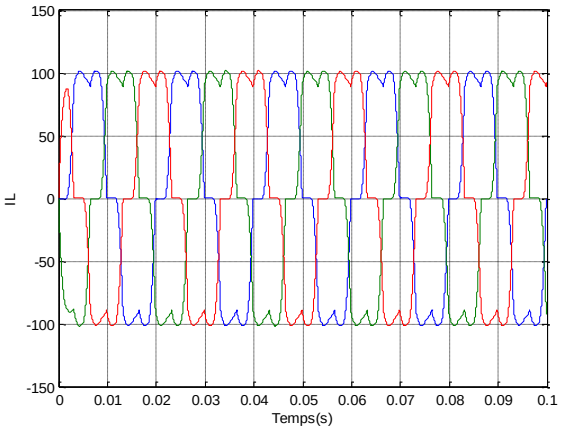

Fig. 9. The load current Il

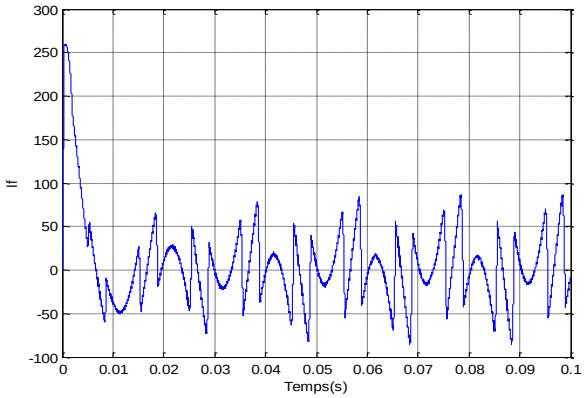

Fig.10. The PAPF current If

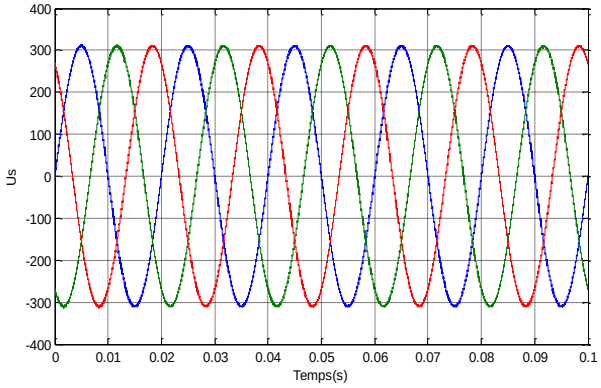

Fig.11. The supply voltage Us

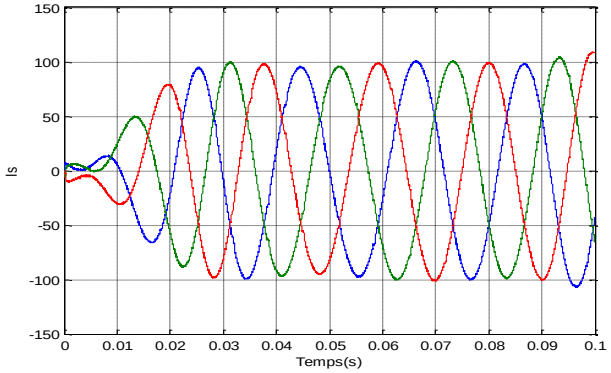

Fig.12. The supply current Is

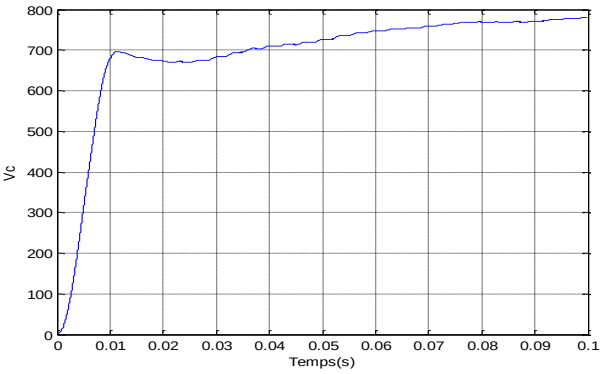

Fig.13. The Vdc bus voltage of the PAPF

The harmonic spectrum of the load and the supply current is shown in Figure 14 and Figure 15 respectively.

The total harmonic distortion (THD) of the source current is decreased from 21.86% befor compensation to 1.99%

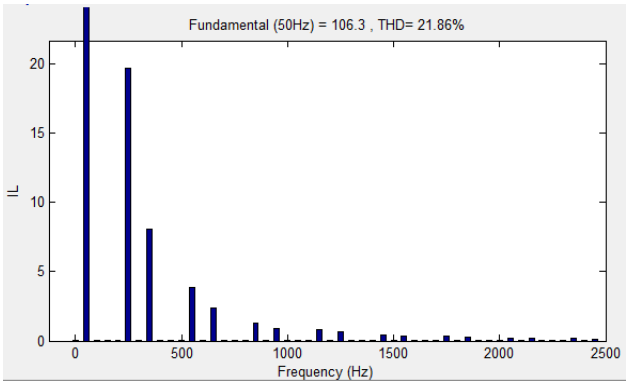

Fig.14. Load current spectrum

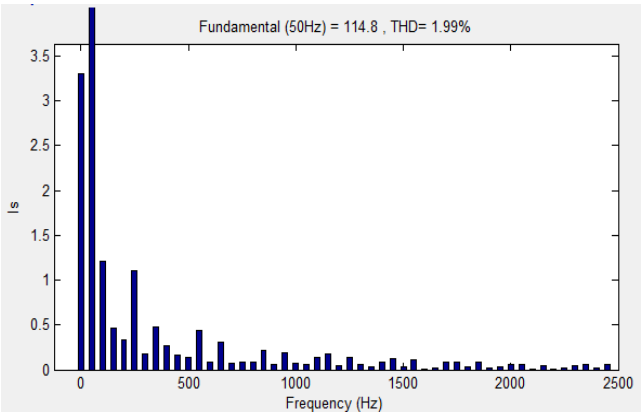

Fig.15. Source current spectrum

From Figure 7 to figure 13, it is observed that the RL nonlinear load current is non-sinusoidal in wave shape. A three-phase R-L nonlinear load current exhibits a step wave-shape and there is an instantaneous change from one step to another step. There is also a period of discontinuity (zero current) near zero crossing points where the load current changes from positive half cycle to negative half cycle and vice versa. Both of the factors that are mentioned required an instantaneous compensation of the load harmonics, but the delay in the compensation of NSVPWM control results switching ripples in the supply currents. It is also essential to find out that, why the NSVPWM algorithm of PAPF suffers from the problem of switching ripples.

It is found from this figure that the supply current exhibit ripples free sinusoidal shape. That the voltage is same (Vc1 = Vc2) for both halves of the center tapped Vdc bus capacitor used in the PAPF circuit. The dc bus voltage of the PAPF circuit is found to be self-supporting.

V. CONCLUSION

In this paper an active filter was modeled and simulated insured for adequate control in real time harmonic currents in MATLAB/SIMULINK.

The objective of this project was completed with a review of theorems and concepts of electric power in non sinusoidal conditions.

In this article, we presented the model of the voltage inverter three structure levels NPC. From this model, it was found that the three-level inverter.

Then we presented the organization chart that summarizes the six-step NSVPWM proposed.

The simulation results have shown that the VA output voltage harmonics are grouped into families centered around multiple frequencies of the switching frequency.

VI. ACKNOWLEDGMENTS

A short section can be written between the conclusion and the references Acknowledgments give an opportunity for the authors to thank people who helped them to prepare the paper.

VII. REFERENCES

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