

Novel Multilevel Inverter Application for Electric Traction

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Abstract - An efficient, cost-effective and small power converter is a prerequisite for industrial applications such as electric traction. Multilevel inverters have a promising role in industrial applications and due to their high number of devices, size, cost and control, their complexities have limited their market penetration. To remedy the disadvantages of multilevel inverters the next-generation topologies under the name of reduced number of switches appeared. In this paper, a new 11-level inverter is proposed by reducing the number of controllable switches, they consist of two stages: the first stage is a half H-bridge connected to stage 2, which consists of a three-level inverter with asymmetric DC sources, the proposed topologist can be extensible in 15-level, 23-level and 17 level inverters. The proposed 11-level inverter is tested by simulations on an inductive load and a controlled PMSM electric vehicle actuator. The obtained results show the effectiveness of the proposed topology.

Keywords — multilevel inverter, 11-level inverter, field-oriented control, PMSM, 15-level inverter, 23-level inverter, 17-level inverter.

I. INTRODUCTION

Multilevel inverters, are critical electronic devices used in the conversion of electrical energy. They are essential in a variety of applications, including power electronics, industrial processes, renewable energy systems, and power transmission. Multilevel inverters are characterized by their ability to provide high-quality sinusoidal output voltage while minimizing harmonic distortion and increasing energy efficiency [1].

Multilevel inverters, as opposed to standard two-level inverters that use a single switch to flip between voltage levels, use numerous voltage levels to create a sinusoidal waveform. This method has a number of major advantages, including less electromagnetic interference, less stress on electronic components, increased power management capabilities, and improved output voltage quality [2].

Over the years, multilevel inverters have gained popularity due to their high performance, reliability, and adaptability to various applications. They are commonly used in motor

drive systems, renewable energy sources, power converters, electric vehicles, and many other industrial sectors [3].

The topology introduced in [4] distinguishes itself among the various scrutinized inverter architectures due to its inherent simplicity. This configuration significantly reduces the count of electrical components, employing a mere 8 IGBTs and 8 diodes. This user-friendly design bears the potential to yield cost savings while effectively addressing the specific requirements of designated applications.

Likewise, the design in [5] is characterized by simplicity, featuring 7 IGBTs and 10 diodes. However, the augmented number of diodes may exert influence on both performance and pricing considerations.

The proposed topologies in [6] fall within an intermediate complexity range, each integrating 10 IGBTs and 10 diodes. This consistent component count facilitates the streamlining of inverter administration and control processes, rendering them well-suited for specific applications.

Conversely, the configuration detailed in [7] entails a complex assembly, comprising 17 IGBTs and 17 diodes. The complexity is justified by specific performance requirements; however, this may result in elevated costs and intricate design considerations.

In [8], [9], and [10], all topologies are characterized by a relatively high count of IGBTs and diodes. These designs may contribute to heightened complexity and increased costs.

The 7-level inverter proposed in [11] features 10 IGBTs and 10 diodes, categorizing it within the moderate complexity spectrum.

Finally, [12] proposes a sophisticated arrangement, encompassing 12 IGBTs and 12 diodes. This configuration, while more intricate in terms of components, can be justified based on the unique requirements of the application.

This paper presents proposed topologies of 11-level inverters, offering a unique configuration. The topology exhibits a significant reduction in the number of controllable switches and voltage sources. The designs feature seven controlled switches and three strategically positioned asymmetric voltage sources, enabling the generation of all possible combinations to achieve the maximum output level.

The paper is organized into four primary sections. Section 2 and 3 provides a comprehensive explanation of the proposed topologies, outlining their functionality and potential for generalization in terms of levels or phases. Section 4 conducts a comparative analysis between the various 11-level inverter topologies and other recently developed configurations. The fifth section demonstrates the application of the proposed topologies in an electric traction drive employing a permanent magnet synchronous machine (PMSM), presenting results and insightful commentary. Finally, Section 5 summarizes the conclusions drawn from the research.

II. PROPOSED TOPOLOGY DESCRIPTION

The topology proposed in figure 1 consists of two stages: the first stage is a half H-bridge consisting of two switches K6 and K7 and a DC

source of value of 4 Vdc connected to stage 2, which consists of a three-level inverter with three switches K₁, K₂ and K₃ and two sources of value of vdc : these two structures are interconnected by two switches K4 and K5 so as to generate the eleven levels (5vdc, 4vdc, 3vdc, 2vdc, vdc, 0, -vdc, -2vdc, -3vdc, -4vdc, -5vdc).

The structure shown in figure 2 is an extension of the first structure on the side of stage 2 so as to have fifteen levels which is done with the addition of a single switch K8 and a continuous source of value, the same for the topology of figure 3; the difference is in the configuration of the switches K8 and the continuous source vdc which is done on stage 1, which gives us seventeen levels. The third structure which is shown in figure 4 is also an extension of the first structure which has been modified in the two stages (half-bridge h and the three-level inverter); two switches k8 and k9 and two DC sources of value vdc and 4vdc the switch k8 and the DC source will be added in stage 1 and the other (K9 and DC source with the value of 4Vdc) are inserted in stage 2, which have generated twenty-three levels.

For the detailed study, the eleven-level structure will be chosen for the next step, all extension is illustrated in figure 2. All states of each topology (11-level, 15-level, 23-level and 17-level) are summarized in table 1, 2, 3 and 4.

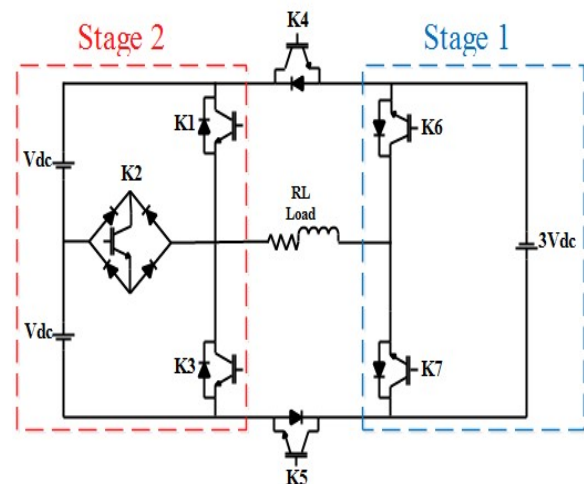


Fig. 1. Proposed topology of 11- level inverter.

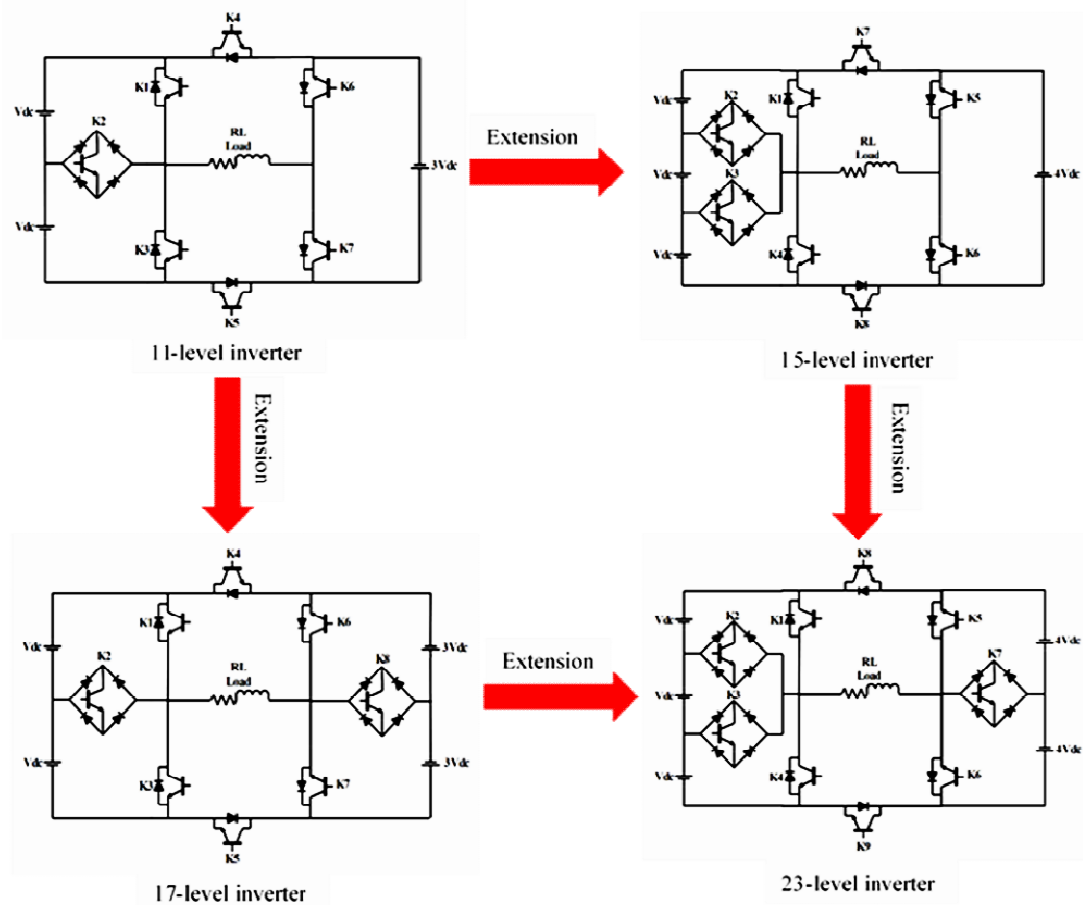


Fig. 2. Extension of proposed 11-level inverter.

TABLE 1. SWITCHING TABLE OF SWITCHES FOR A PHASE OF THE PROPOSED TOPOLOGY 11-LEVEL.

K1	K2	K3	K4	K5	K6	K7	V _{ao}
1	0	0	0	1	1	0	5V _{dc}
0	1	0	0	1	1	0	4V _{dc}
0	0	1	0	1	1	0	3V _{dc}
1	0	0	0	1	0	1	2V _{dc}
0	1	0	0	1	0	1	V _{dc}
1	0	0	1	0	1	0	0
0	0	1	0	1	0	1	0
0	1	0	1	0	1	0	-V _{dc}
0	0	1	1	0	1	0	-2V _{dc}
1	0	0	1	0	0	1	-3V _{dc}
0	1	0	1	0	0	1	-4V _{dc}

III. OPERATING OF PROPOSED 11 LEVEL TOPOLOGY

In order to more explain the operating of the proposed topology, it is imperative to define the eleven-level of the output voltage V_{ao} . The different possible level could be generated, by the

association of the two topologies shown in Figure 1, are eleven: (5v_{dc}, 4v_{dc}, 3v_{dc}, 2v_{dc}, v_{dc}, 0, -v_{dc}, -2v_{dc}, -3v_{dc}, -4v_{dc} and -5v_{dc}, as illustrated in Figure 2. For this purpose, the control process, presented in Table 1 should be followed. One can see that each level is synthesized by a combination of the seven switches where three of them are ON and others are OFF.

All possible switching combinations are analyzed in this section, as shown in Figure 3. There can be only one switching combination for each output voltage level except mode 0. The current flows of these eleven different modes of the proposed inverter are shown in Figure 3, where the line in red means the conduction path.

(1) Mode 1 Positive output level 5V_{dc}: In the switching case of Figure 3 (1), the total voltage applied to the load is equal to 5V_{dc} when the three DC sources are connected in series. For the

5Vdc voltage the switches K1 K5 and K6 must be ON and K2, K3, K4 and K7 are OFF.

(2) Mode 2 Positive output level 4Vdc: In the switching state of Figure 3(i), the total voltage applied to the load is equal to 4Vdc. For this amplitude voltage the switches K2, K5 and K6 are ON where and K1, K3, K4 and K7 are OFF.

(3) Mode 3 Positive output level 3Vdc: In the case of configuration of Figure 3(g), K3, K5 and K6 are ON where K1, K2, K4 and K7 are OFF, the total voltage applied to the load is equal to Vdc

(4) Mode 4 Positive output level 2Vdc: In the switching state of Figure 3(e), the total voltage applied to the load is equal to 2Vdc. For this amplitude voltage the switches K1, K5 and K7 are ON where and K2, K3, K4 and K6 are OFF.

(5) Mode 5 Positive output level 1Vdc: In the switching state of Figure 3(c), the total voltage applied to the load is equal to 1Vdc. For this amplitude voltage the switches K2, K5 and K7 are ON where and K1, K3, K4 and K6 are OFF.

(6) Mode 0 Zero output level (Figure 3 (a) and (b)): To get zero voltage switches K1, K4 and K6 must be ON and K2, K3, K5 and K7 are OFF. or switches K3, K5 and K7 must be ON and K1, K2, K4 and K6 are OFF

(7) Mode 6 Negative output level -1Vdc (Figure 3(d)): -Vdc is applied to the load in this switching case, switches K2, K4 and K6 are ON where K1, K3, K5 and K7 are OFF.

(8) Mode 7 Negative output level -2Vdc: In the switching state of Figure 3 (f), the total voltage applied to the load is equal to -2Vdc. for this amplitude voltage the switches K3, K4 and K6 are ON where K1, K2, K5 and K7 are OFF.

(9) Mode 8 negative output level -3Vdc: In the switching case of Figure 3 (h), the total voltage applied to the load is equal to -3Vdc. for this amplitude voltage the switches K1, K4 and K7 must be ON and K2, K3, K5 and K6 are OFF

(10) Mode 9 Negative output level -4Vdc: In the switching state of Figure 3 (j), the total voltage applied to the load is equal to -4Vdc. for this amplitude voltage the switches K2, K4 and K7 are ON where K1, K3, K5 and K6 are OFF.

(11) Mode 10 Negative output level -5Vdc (Figure 3(l)): -Vdc is applied to the load in this switching case, switches K3, K4 and K7 are ON where K1, K2, K5 and K6 are OFF.

TABLE 2. SWITCHING TABLE OF SWITCHES FOR A PHASE OF THE PROPOSED TOPOLOGY 15-LEVEL.

K1	K2	K3	K4	K5	K6	K7	K8	Vao
1	0	0	0	1	1	0	0	7vdc
0	1	0	0	1	1	0	0	6vdc
0	0	0	0	1	1	0	1	5vdc
0	0	1	0	1	1	0	0	4vdc
1	0	0	0	1	0	1	0	3vdc
0	1	0	0	1	0	1	0	2vdc
0	0	0	0	1	0	1	1	vdc
0	0	1	0	1	0	1	0	0
1	0	0	1	0	1	0	0	0
0	1	0	1	0	1	0	0	-vdc
0	0	0	1	0	1	0	1	-2vdc
0	0	1	1	0	1	0	0	-3vdc
1	0	0	1	0	0	1	0	-4vdc

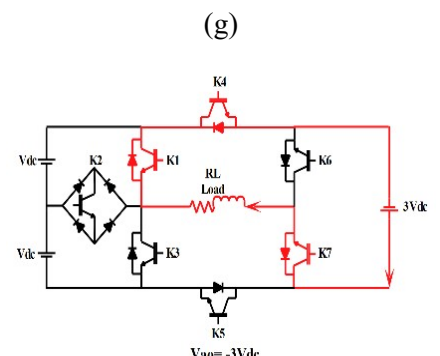
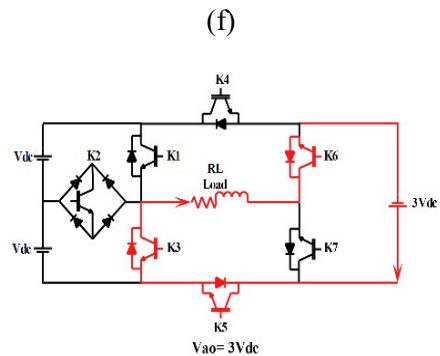
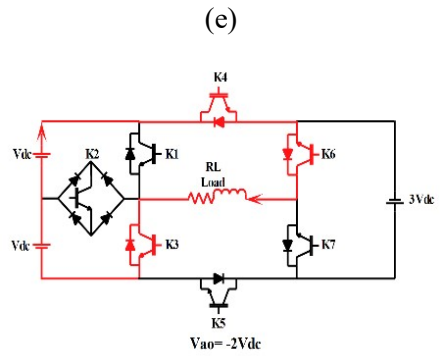
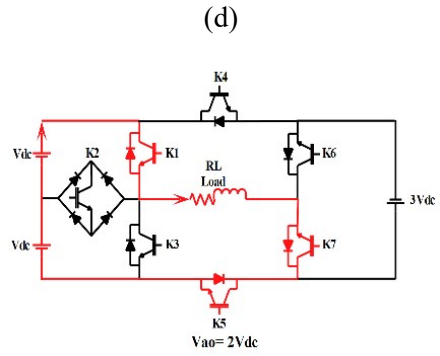
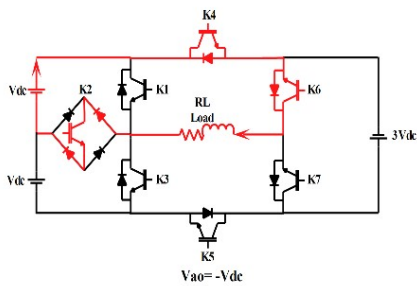
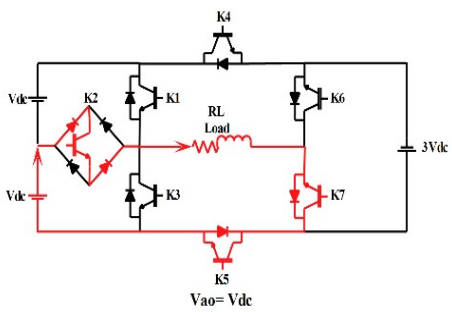
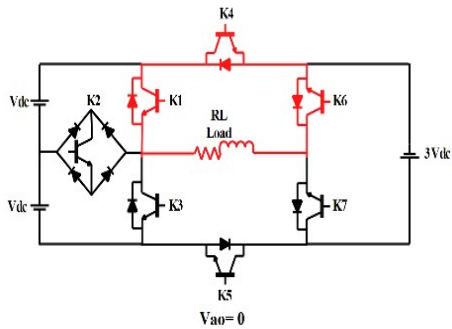
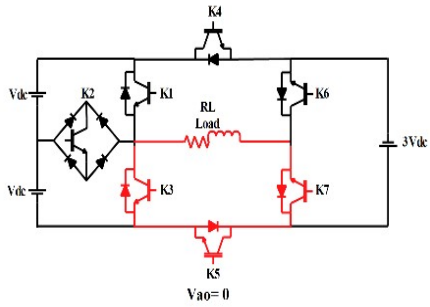
TABLE 3. SWITCHING TABLE OF SWITCHES FOR A PHASE OF THE PROPOSED TOPOLOGY 23-LEVEL.

K 1	K 2	K 3	K 4	K 5	K 6	K 7	K 8	K 9	Vao
1	0	0	0	1	1	0	0	0	11vdc
0	1	0	0	1	1	0	0	0	10vdc
0	0	0	0	1	1	0	1	0	9vdc
0	0	1	0	1	1	0	0	0	8vdc
1	0	0	0	1	0	0	0	1	7vdc
0	1	0	0	1	0	0	0	1	6vdc
0	0	0	0	1	0	0	1	1	5vdc
0	0	1	0	1	0	0	0	1	4vdc
1	0	0	0	1	0	1	0	0	3vdc
0	1	0	0	1	0	1	0	0	2vdc
0	0	0	0	1	0	1	1	0	vdc
0	0	1	0	1	0	1	0	0	0
1	0	0	1	0	1	0	0	0	0
0	1	0	1	0	1	0	0	0	-vdc
0	0	0	1	0	1	0	1	0	-2vdc
0	0	1	1	0	1	0	0	0	-3vdc
1	0	0	1	0	0	0	0	1	-4vdc
0	1	0	1	0	0	0	0	1	-5vdc
0	0	0	1	0	0	0	1	1	-6vdc
0	0	1	1	0	0	0	0	1	-7vdc
1	0	0	1	0	0	1	0	0	-8vdc
0	1	0	1	0	0	1	0	0	-9vdc
0	0	0	1	0	0	1	1	0	-10vdc
0	0	1	1	0	0	1	0	0	-11vdc

TABLE 4. SWITCHING TABLE OF SWITCHES FOR A PHASE OF THE PROPOSED TOPOLOGY 17-LEVEL.

K1	K2	K3	K4	K5	K6	K7	K8	vao
1	0	0	0	1	1	0	0	8vdc
0	1	0	0	1	1	0	0	7vdc
0	0	1	0	1	1	0	0	6vdc
1	0	0	0	1	0	0	1	5vdc
0	1	0	0	1	0	0	1	4vdc
0	0	1	0	1	0	0	1	3vdc
1	0	0	0	1	0	1	0	2vdc
0	1	0	0	1	0	1	0	Vdc
1	0	0	1	0	1	0	0	0

0	0	1	0	1	0	1	0	0
0	1	0	1	0	1	0	0	-vdc
0	0	1	1	0	1	0	0	-2vdc
1	0	0	1	0	0	0	1	-3vdc
0	1	0	1	0	0	0	1	-4vdc
0	0	1	1	0	0	0	1	-5vdc
1	0	0	1	0	0	1	0	-6vdc
0	1	0	1	0	0	1	0	-7vdc
0	0	1	1	0	0	1	0	-8vdc



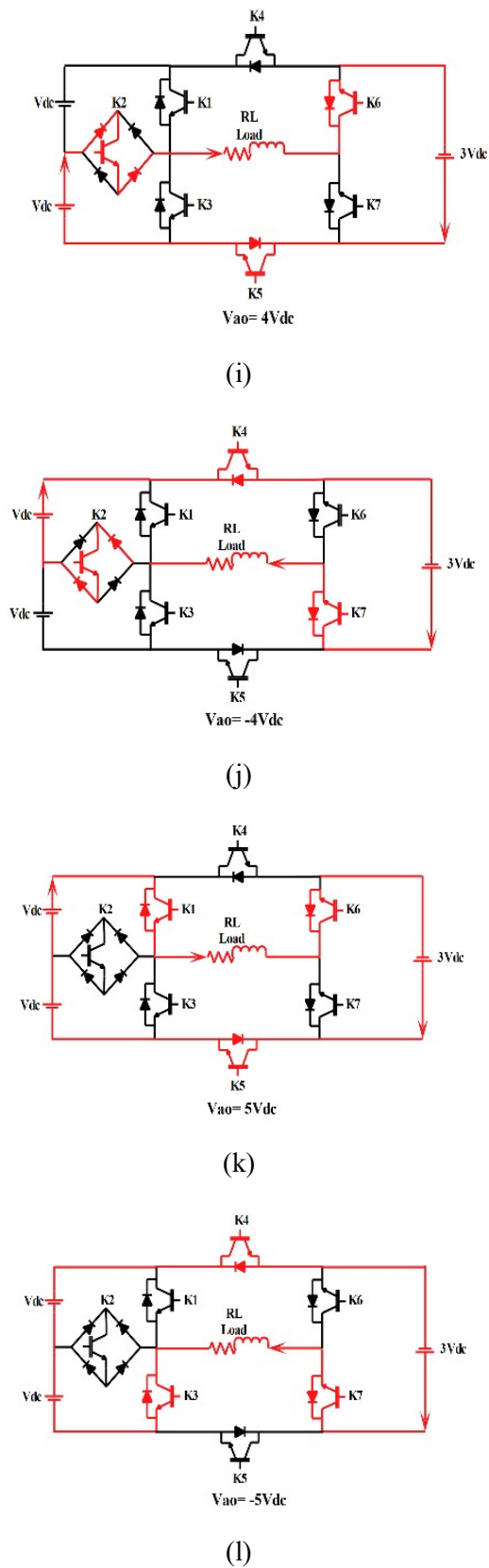


Fig. 3. Operating modes of the proposed single-phase 11-level inverter.

IV. COMPARISON

The proposed topology is compared to the most relevant ones as summarized in table 5. It could be concluded that the proposed topology requires has optimized the number of controllable switches which will reduce the commutation losses and enhance system efficiency. In addition to that, the control of the proposed topology will be easier. The proposed new 11-level inverter topology retains all the advantages of the conventional multilevel inverter and eliminates their disadvantages.

TABLE 5. COMPARISON WITH RECENT DIFFERENT 11-LEVEL INVERTERS.

Structures	Number of level	IGBTs	Diodes	Sources
[4]	7	8	8	3
[5]	9	7	10	3
[6]	11	12	12	3
[7]	9	17	17	4
[8]	11	14	14	5
[9]	11	12	12	4
[10]	11	12	12	5
[11]	7	10	10	4
[12]	7	12	12	5
Proposed topology	11	7	10	3

V. SIMULATION OF PROPOSED TOPOLOGY

The proposed three-phase 11-level inverter (figure 4) controlled by using POD-PWM strategy [13], in POD-PWM, multiple triangular carrier signals are aligned with a reference sinusoidal signal to generate pulses, are integrated into a field-oriented control strategy aimed at regulating the speed of a PMSM, thereby facilitating the traction needs of an electric vehicle comprehensive insight into this FOC control strategy, refer to [14-15]. To validate the performance of the overall system, comprising the inverter and the PMSM, simulations were conducted using MATLAB Simulink. The simulation results, depicted in Figures 5, were obtained with a switching frequency of 10 kHz, providing essential details for a comprehensive understanding of the system's behavior and performance.

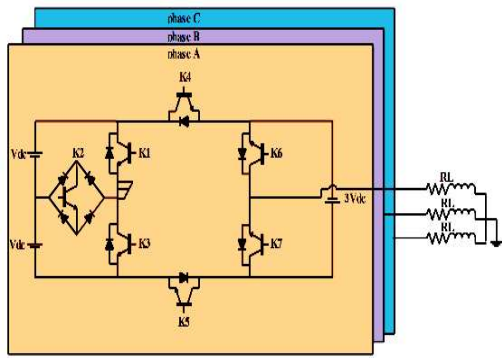
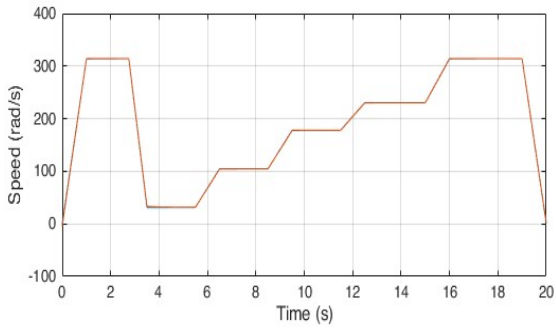
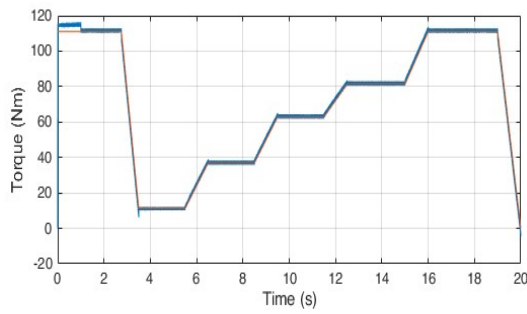


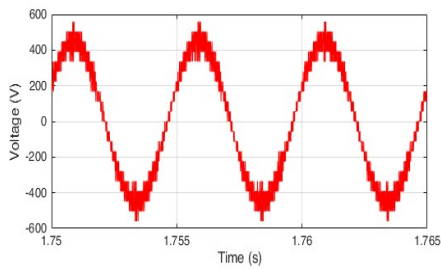
Fig. 4. Proposed three phase 11-level inverter.



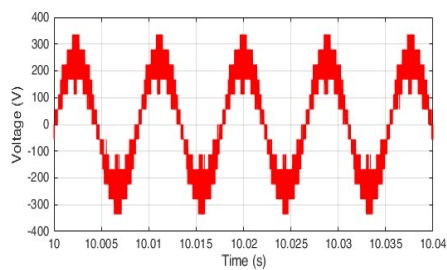
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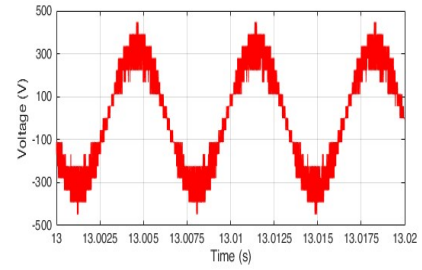
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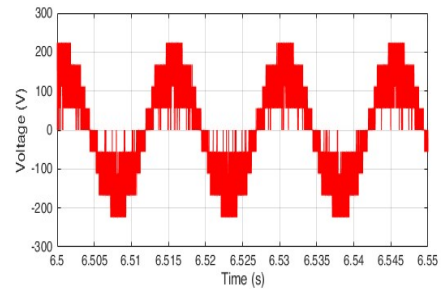
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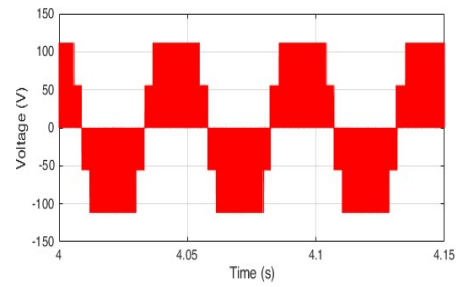
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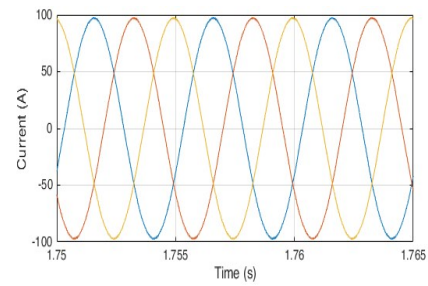
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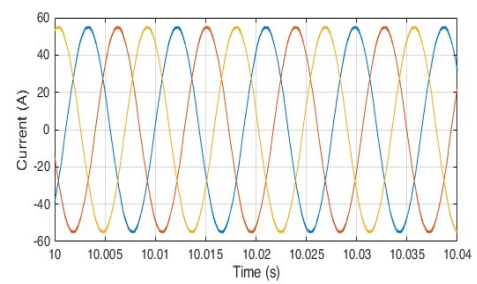
(f)



(g)



(h)



(i)

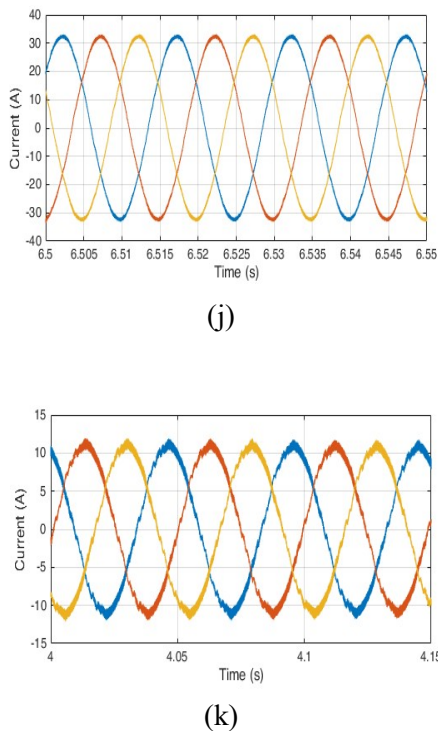


Fig. 5. FOC control simulation results.

To evaluate the functionality of the proposed 11-level inverter to generate different voltage levels under various operating conditions, we established specific speed and load cycles as shown in Figure 5(a-b). Figure 5(a) shows that the motor speed consistently adheres to the designated set point throughout the cycle. However, Voltage levels and frequency vary significantly depending on motor speed, resulting in different voltage waveforms as shown in Figure 5 (c, d, e, f and g), As the motor speed increases, we observe an increase in voltage levels and a variation in frequency. It is essential to note that the 11 levels achievable in the proposed inverter topology is achieved when the motor reaches its synchronous speed of 314 rad/s (figure 5 (c)).

The various current amplitudes corresponding to variations in the imposed load. The quality of both voltage and current waveforms is presented in Figure 5 (h, i, j and k). Notably, the quality of the current waveform directly influences the torque generated, reaching its peak value at 111 Nm, as exemplified in Figure 5 (b). These comprehensive simulations provide valuable information on the performance of the proposed

topology in several scenarios, thus reaffirming its effectiveness.

VI. CONCLUSION

This paper introduces a novel 11-level inverter topology capable of yielding three distinct inverter configurations: 15-level, 17-level, and 23-level inverters, achieved through a reduction in component count. This reduction offers notable advantages, including cost savings, enhanced system reliability, and simplified control strategies. The proposed 11-level inverter stands out for its capacity to generate high-quality voltage waveforms, meeting the stringent requirements of electric vehicles. This innovative topology holds significant promise for electric traction applications, combining advantages such as reduced component count and superior voltage waveform quality. The associated switch counts for each inverter are as follows: 11-level (7 switches), 15-level (8 switches), 17-level (8 switches), and 23-level (9 switches).

VII. REFERENCES

- [1] Jahan, H. K., Panahandeh, F., Abapour, M., & Tohidi, S. (2017). Reconfigurable multilevel inverter with fault-tolerant ability. *IEEE Transactions on Power Electronics*, 33(9), 7880-7893.111
- [2] DE, S., BANERJEE, D., GOPAKUMAR, K., et al. Multilevel inverters for low-power application. *IET Power Electronics*, 2011, vol. 4, no 4, p. 384-392.
- [3] ESCALANTE, Miguel F., VANNIER, J.-C., et ARZANDÉ, Amir. Flying capacitor multilevel inverters and DTC motor drive applications. *IEEE Transactions on Industrial Electronics*, 2002, vol. 49, no 4, p. 809-815.
- [4] BALAMURUGAN, C. R. et NATARAJAN, S. P. Assessment of multilevel inverter using embedded and digital controller for various loads. *International Journal of Energy Technology and Policy*, 2015, vol. 11, no 3, p. 274-293.
- [5] ODEH, Charles Ikechukwu, OBE, Emeka S., et OJO, Olorunfemi. Topology for cascaded multilevel inverter. *IET Power Electronics*, 2016, vol. 9, no 5, p. 921-929.
- [6] BASSI, Hussain et RAWA, Muhyaddin. A new hybrid multilevel inverter with extended number of voltage steps. *International Journal of Electrical and Electronic Engineering & Telecommunications*, 2020, vol. 9, no 4, p. 223-230.
- [7] SAMIZADEH, Mehdi, YANG, Xu, KARAMI, Bagher, et al. A new topology of switched-capacitor multilevel inverter with eliminating leakage current. *IEEE Access*, 2020, vol. 8, p. 76951-76965.

- [8] KARTHIKEYAN, Vasudevan, JAMUNA, Venkatesan, et JAMES, Abisha. Multilevel Inverter for Hybrid Energy Generation System. *Applied Mechanics and Materials*, 2014, vol. 622, p. 127-131.
- [9] LEE, Sze Sing, LIM, Chee Shen, et LEE, Kyo-Beum. Novel active-neutral-point-clamped inverters with improved voltage-boosting capability. *IEEE Transactions on Power Electronics*, 2019, vol. 35, no 6, p. 5978-5986.
- [10] BANAEI, Mohamad Reza et SALARY, Ebrahim. New multilevel inverter with reduction of switches and gate driver. *Energy Conversion and Management*, 2011, vol. 52, no 2, p. 1129-1136.
- [11] LEE, Sze Sing et LEE, Kyo-Beum. Dual-T-type seven-level boost active-neutral-point-clamped inverter. *IEEE Transactions on Power Electronics*, 2019, vol. 34, no 7, p. 6031-6035.
- [12] YADAV, Apurv Kumar, GOPAKUMAR, K., UMANAND, Loganathan, et al. A hybrid 7-level inverter using low-voltage devices and operation with single DC-link. *IEEE Transactions on Power Electronics*, 2019, vol. 34, no 10, p. 9844-9853.
- [13] Kerrouche, F., Tazerart, F., Taib, N. (2020). Novel topology of a multilevel inverter dedicated to electric traction drive. *European Journal of Electrical Engineering*, Vol. 22, No. 3, pp. 255-263. <https://doi.org/10.18280/ejee.220306>
- [14] F. Kerrouche et al., "A New Three-Phase Multilevel Inverter for Electric Drive," 2023 1st International Conference on Circuits, Power and Intelligent Systems (CCPIS), Bhubaneswar, India, 2023, pp. 1-7, doi: 10.1109/CCPIS59145.2023.10291315
- [15] F. Kerrouche, F. Tazerart, N. Taib, A. Oubelaid, M. F. Ansari and M. B., "Novel Three Phases Compact Multilevel Inverter For Electric Vehicles," 2023 IEEE 3rd International Conference on Applied Electromagnetics, Signal Processing, & Communication (AESPC), Bhubaneswar, India, 2023, pp. 1-6, doi: 10.1109/AESPC59761.2023.10390493